IN THE CLAIMS

Please amend the claims as follows:

Claims 1-20 (Canceled):

Claim 21 (Currently Amended): An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and

a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the ~~first~~ second base layer a channel electrically connecting the source layer and the ~~second~~ first base layer,

wherein a voltage transiently applied to said device is larger than a static breakdown voltage between the source and the drain when a rated current is turned off under a condition, said condition being that said device is connected to an inductance load without using a protective circuit.

Claim 22 (Previously Presented): The insulated gate semiconductor device according to claim 21, wherein the inductance load is from 1 μH to 1 mH under said condition.

Claim 23 (Previously Presented): The insulated gate semiconductor device according to claim 21, wherein a thickness of the first base layer is at most 70 μm.

Claim 24 (Previously Presented): The insulated gate semiconductor device according to claim 21, wherein a total impurity dose of the drain layer is at most $5x10^{13}$ cm^{-2}.

Claim 25 (Previously Presented): The insulated gate semiconductor device according to claim 21, wherein a thickness of the drain layer is at most 0.5 μm.

Claim 26 (Currently Amended): An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and

a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the ~~first~~ second base layer a channel electrically connecting the source layer and the ~~second~~ first base layer,

wherein a voltage transiently applied to said device decreases gradually as a drain current decreases after a rated current is turned off, said voltage transiently applied to said device rising when the rated current is turned off under a condition, said condition being that said device is connected to an inductance load without using a protective circuit.

Claim 27 (Previously Presented): The insulated gate semiconductor device according to claim 26, wherein the voltage transiently applied to said device is larger than a static breakdown voltage between the source and the drain when the rated current is turned off under said condition, and the inductance load is from 1 μH to 1 mH under said condition.

Claim 28 (Previously Presented): The insulated gate semiconductor device according to claim 26, wherein a thickness of the first base layer is at most 70 μm.

Claim 29 (Previously Presented): The insulated gate semiconductor device according to claim 26, wherein a total impurity dose of the drain layer is at most $5x10^{13}$ cm^{-2}.

Claim 30 (Previously Presented): The insulated gate semiconductor device according to claim 26, wherein a thickness of the drain layer is at most 0.5 μm.

Claim 31 (Currently Amended): An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and

a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the ~~first~~ second base layer a channel electrically connecting the source layer and the ~~second~~ first base layer,

wherein a voltage transiently applied to said device is larger than a static breakdown voltage between the source and the drain and decreases gradually as a drain current decreases after a rated current is turned off, said transiently applied voltage rising when the rated current is turned off under a condition, said condition being that said device is connected to an inductance load without using a protective circuit.

Claim 32 (Previously Presented): The insulated gate semiconductor device according to claim 31, wherein said voltage transiently applied to said device is larger than said static breakdown voltage between the source and the drain when said rated current is turned off under said condition, and the inductance load is from 1 μH to 1 mH under said condition.

Claim 33 (Previously Presented): The insulated gate semiconductor device according to claim 31, wherein a thickness of the first base layer is at most 70 μm.

Claim 34 (Previously Presented): The insulated gate semiconductor device according to claim 31, wherein a total impurity dose of the drain layer is at most $5x10^{13}$ cm^{-2}.

Claim 35 (Previously Presented): The insulated gate semiconductor device according to claim 31, wherein a thickness of the drain layer is at most 0.5 μm.

Claim 36 (New): The insulated gate semiconductor device according to claim 21, further comprising:

a buffer layer of the first conduction type provided between the first base layer and the drain layer, the impurity concentration of the buffer layer is higher than that of the first base layer.

Claim 37 (New): The insulated gate semiconductor device according to claim 26, further comprising:

a buffer layer of the first conduction type provided between the first base layer and the drain layer, the impurity concentration of the buffer layer is higher than that of the first base layer.

Claim 38 (New): The insulated gate semiconductor device according to claim 31, further comprising:

a buffer layer of the first conduction type provided between the first base layer and the drain layer, the impurity concentration of the buffer layer is higher than that of the first base layer.